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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/699,947	10/30/2000	Edmund J. Kelly	TRANS04D	8830

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EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/699,947	KELLY ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/15/2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-9,12,13 and 18-20* is/are pending in the application.

4a) Of the above claim(s) *4,10,11 and 14-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-9,12,13 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Response to Amendment

1. This office action is in response to Applicant's communication filed December 15, 2005. This amendment has been entered and carefully considered. Claims 1-3, 5-9, 12-13 and 18-20 remain pending in the application. Claims 4, 10-11 and 14-17 have been cancelled.

Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5-9, 12-13 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore et al. (USPN: 5,437,017), hereinafter Moore, in view of IBM TDB, May 1994, Vol. 37, Issue 5, pages 249-250; hereinafter IBM 37.

As per claim 1, Moore teaches the invention as claimed including a method and system for protecting memory from being written in a computer [6] which includes a single host processor designed to execute instructions of a host instruction set and software synchronization utilized for instruction/data translation and TLB coherency (e.g. see column 2, lines 36-37) comprises hardware means having a translation look-aside buffer with a storage position in each storage location included in each processor for translating an effective or virtual address to a real address within system memory (e.g. see figure 1, column 4, lines 19 et seq.); software means responding an indication once the memory address has been written is taught as the software implementation of a translation look-aside buffer invalidate (TLBI) instruction or by software synchronization throughout the multiprocessor data processing system (e.g. see column 2, lines 36-37; figure 5, column 8, lines 32 et seq.). Moore discloses the invention as claimed except means for indicating whether memory address stores target instruction which has been translated into host instruction. IBMTDB 37, in its teaching of the use of the SYNC instruction to synchronize completion of Translation Lookaside Buffer Invalidate in Multiprocessor system, discloses the means for indicating whether memory address stores target instruction which has been translated into host instruction as being equivalent to the SYNC operation instruction

signal received from the receiving processor after broadcasting of the TBLI instruction for indicating of whether the instruction has been translated/ executed within the local receiving processor (TBLI instruction has taken effect throughout the SMP environment; e.g. see disclosure text). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to utilize the means for indicating whether memory address stores target instruction which has been executed/translated into host instruction (being equivalent to the SYNC operation signal) as taught and being disclosed in the IBM TDB 37 for that of Moore's system in order to arrive at Applicant's current invention. In doinq so, it would enhance system reliability and throughput by allowing the host in Moore's system to quickly and uniformly execute instructions wherein only instructions which has been translated from target into host instruction can be executed, therefore being advantageous.

As per claim 2, Moore further discloses the memory management unit 34 (hardware means) comprises look-aside buffer 40 having plurality of storage locations for virtual addresses and associated physical addresses, and a storage position in each storage location (e.g. see figure 32 column 6, lines 22 et seq.);

As per claim 3, software means for invalidating host instruction translated from target instructions stored at the

memory address is clearly taught by Moore as the software synchronization throughout the multiprocessor data processing system, also by the software implementation of a translation look-aside buffer invalidate (TLBI) (e.g. see column lines 36- figure column lines 32 et seq.; also see abstract, column 3, lines 12 et seq.);

As per claim 5, Moore discloses software means for protecting against writing the memory address removes translations associated with the memory address taught as software synchronization and means for purging instructions within the plurality of processors for achieving coherency (e.g. see column 2, lines 36-37; and claims 12 and 13);

As per claim 6, Moore further discloses the memory management unit 34 (hardware means) comprises look-aside buffer 40 having plurality of storage locations for virtual addresses and associated physical addresses, and a storage position in each storage location (e.g. see figure 3; column 6, lines 22 et seq.); software means for protecting against writing the memory address removes translations associated with the memory address is taught as software synchronization and means for purging all instructions within the plurality of processors for achieving coherency (e.g. see column 2, lines 36-37: and claims 12 and 13);

As per claims 7 and 8, see arguments with respect to claim in addition, Moore further discloses hardware means for

generating and exception to a write access ... to a host instruction as being equivalently taught as means for suspending execution of instructions within each of said plurality of processors until coherency is achieved (e.g. see claim 12); Moore also discloses the memory management unit 34 (hardware means) comprises look-aside buffer 40 having plurality of storage locations for virtual addresses and associated physical addresses, (e.g. see figure 1; column 2, lines 7 et seq.; figure 3, column 6, lines 22 et seq.);

As per claim 9, software means responding to an exception to a write will not be utilized before being updated is taught as software synchronization and means for purging all instructions within the plurality of processors for achieving coherency (e.g. see column 2, lines 36-37; and claims 12 and 13); also the processing of a translation look-aside buffer invalidate (TLBI) instruction throughout the multiprocessor data processing system (e.g. see figure 5, column 8, lines 32 et seq.);

As per claims 12 and 13; they encompass the same scope of invention as to that of claim except that they are drafted as method format rather apparatus format, the claims are therefore rejected for the same reasons as being set forth above.

As per claims 18-20, they encompass the same scope of invention as to that of claims 1-3, it should further be noted that the memory controller being claimed in claim 18 in which it

comprises a translation look-aside buffer... etc, is equivalent to the memory management unit (MMU) having a TLB (e.g. see figure and other equivalent elements as detailed in claims 1-3. The claims therefore are rejected for the same reason as set forth above. It should be noted that the concept of target instruction being translated into host instruction wherein code intended for a first target processor is translated into code for running on different host processor which is clearly taught by Moore starting on column 4, lines 19 et seq.; for example, Moore does disclose that if the conditional branch is predicted as "taken" then the target instruction is utilized, otherwise it is purged, and the sequential instruction is retrieved.

4. As per remark, Applicant's counsel asserts that (a) Moore does not teach describe or suggest a single host processor as being claimed, instead Moore discloses multiprocessor (amendment, pages 8-11); and (b) the combination of Moore and IBMTDB 37 fails to teach or suggest the invention as claimed (e.g. pages 11, third paragraph et seq.).

With respect to (a); Examiner would like to emphasize that even though being depicted in figure 1 (Moore's '017) as plural of processors 10, the invention of Moore in fact involves in a single processor (e.g. multiple sub-processors 10 having exact or identical characteristics) wherein a translated host

instruction can be stored in the memory for execution by the processor, it is in the same field of endeavors and solving the same intended purpose as of Applicant's invention (e.g. see Moore's abstract; column 4, lines 8 et seq.). Noting that the processor(s) 10 of Moore is being equivalent in its function as to that of the CPU (figure 10) of Applicant; in addition, the operation of Moore's sub-processors 10 is the same with that of CPU 10 which falls within the changes/ modification without departing from the spirit and scope of Moore's invention as indicated in Moore's column 10, lines 48 et seq.;

With respect to (b), it should be noted that the IBMTDB 37 reference cited by Examiner is solely for teaching of the missing element of means for indicating whether memory address stores target instruction which has been translated into host instruction; it does not teach away nor render Moore inoperable for its intended purpose. Specifically, in considering a 35 USC 103 rejection, it is not strictly necessary that a reference or references explicitly suggest the claimed invention (this is tantamount to a 35 USC 102 reference if the modifications would have been obvious to those of ordinary skill in the art. It has been held that the test of obviousness is not whether the features of a secondary reference may be bodily incorporated into the primary references' structure, nor whether the claimed invention is expressly suggested in any one or all of the

references; rather, the test is what the combined teachings of the reference would have suggested to those of ordinary skill in the art. See In re Keller et al., 208 U.S.P.Q 871. In addition, Examiner further recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). Moore and IBMTDB 37 references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA) 1969. In this case, the IBMTDB 37 reference was used to provide evidence of means for indicating whether memory address stores target instruction which has been translated into host instruction as being equivalent to the SYNC operation instruction signal received from the receiving processor after broadcasting of the TBLI instruction for indicating of whether the instruction has been translated/ executed within the local receiving processor (TBLI instruction has taken effect throughout the SMP environment; e.g. see disclosure text). The combination would

enhance system reliability and throughput by allowing the host in Moore's system to quickly and uniformly execute instructions wherein only instructions which has been translated from target into host instruction can be executed. The 35 USC § 103 rejection based on said combination is therefore deemed to be proper.

5. Applicant's arguments filed December 15, 2005 have been fully considered but they are not deemed to be persuasive.

6. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M..

If attempts to reach the examiner by telephone are

unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see ***http://pair-direct.uspto.gov***. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/March 06, 2006

Tuan V. Thai
PRIMARY EXAMINER
Group 2100